CLAIMS

1. An integrated circuit fabricated by:

forming a first dielectric layer in a manner that varies in the Z-dimension; and

forming a first conductive layer over the first dielectric layer, the first conductive layer also varying in the Z-dimension, the first conductive layer having a length and a width, the length being substantially greater than the width, the first conductive layer being arranged in a substantially straight line along the X-dimension, and the first conductive layer comprising upper segments and lower segments, the upper segments being longer than the lower segments.

2. The integrated circuit recited in claim 1 wherein, in forming the first dielectric layer, the first dielectric layer is arranged in a stepped manner.

3. The integrated circuit recited in claim 1 wherein, in forming the first dielectric layer, the first dielectric layer is arranged in an undulating manner.

4. The integrated circuit recited in claim 1 wherein, in forming the first dielectric layer, the first dielectric layer is arranged in a manner that alternates between trenches and pedestals.

5. An integrated circuit as recited in claim 1 and further fabricated by:

forming a second dielectric layer in a manner that varies in the Z-dimension;

forming a second conductive layer over the second dielectric layer, the second conductive layer also varying in the Z-dimension, the second conductive layer having a length and a width, the length being substantially greater than the width, the second conductive layer being arranged in a substantially straight line along the X-dimension, and the second conductive layer comprising upper segments and lower segments, the upper segments being longer than the lower segments; and

coupling the second conductive layer to the first conductive layer.

6. The integrated circuit recited in claim 5 wherein, in forming the second conductive layer, the upper segments in the first conductive layer are offset 180 degrees from the upper segments in the second conductive layer.

7. The integrated circuit recited in claim 1 wherein, in forming the first conductive layer, the first conductive layer comprises material from the group consisting of copper, aluminum, tungsten, molybdenum, titanium, gold, silver, palladium, a metal silicide, doped polysilicon, or is an alloy whose constituents are from the group.

8. The integrated circuit recited in claim 1 wherein, in forming the first conductive layer, the first conductive layer comprises magnetic material.

9. The integrated circuit recited in claim 8 wherein, in forming the first conductive layer, the magnetic material is from the group consisting of nickel-iron, cobalt-zirconium-tantalum, iron-tantalum-nickel, nickel-iron-rhenium, and ferro-silicon.

10. The integrated circuit recited in claim 8 wherein, in forming the first conductive layer, the magnetic material is from the group consisting of iron, nickel, cobalt, manganese, zinc, zirconium, tantalum, rhenium, silicon, and the rare earth elements, or is an alloy whose constituents are from the group.

11. An integrated circuit package fabricated by:

forming at least one multi-level inductive element on a substrate in a serpentine pattern comprising at least two rows, wherein each row comprises upper conductive segments and lower conductive segments, and in at least one row the upper conductive segments are longer than the lower conductive segments; and

mounting an integrated circuit on the substrate.

12. The integrated circuit package recited in claim 11 wherein, in forming, the upper conductive segments and the lower conductive segments are arranged in a stepped manner.

13. The integrated circuit package recited in claim 11 wherein, in forming, the upper conductive segments and the lower conductive segments are arranged in an undulating manner.

14. The integrated circuit package recited in claim 11 wherein, in forming, the upper conductive segments in one row are offset 180 degrees from the upper conductive segments in an adjacent row.

15. The integrated circuit package recited in claim 11 wherein, in forming, the at least one multi-level inductive element comprises at least one layer of magnetic material.

16. An integrated circuit component fabricated by:

forming a substrate; and

forming at least one multi-level inductive element on the substrate in a serpentine pattern comprising at least two rows, wherein each row comprises upper conductive segments and lower conductive segments, and in at least one row the upper conductive segments are longer than the lower conductive segments.

17. The integrated circuit component recited in claim 16 wherein, in forming the substrate, the substrate is formed of material from the group consisting of silicon, germanium, gallium arsenide, polyimide, organic material, a printed circuit board, glass, quartz, and ceramic.

18. The integrated circuit component recited in claim 16 wherein, in forming the at least one multi-level inductive element, the upper conductive segments and the lower conductive segments are arranged in a stepped manner.

19. The integrated circuit component recited in claim 16 wherein, in forming the at least one multi-level inductive element, the upper conductive segments and the lower conductive segments are arranged in an undulating manner.

20. The integrated circuit component recited in claim 16 wherein, in forming the at least one multi-level inductive element, the upper conductive segments in one row are offset 180 degrees from the upper conductive segments in an adjacent row.

21. The integrated circuit component recited in claim 16 wherein, in forming the at least one multi-level inductive element, the at least one multi-level inductive element comprises at least one layer of magnetic material.

22. An integrated circuit package fabricated by:

forming a substrate;

forming at least one multi-level inductive element on the substrate in a serpentine pattern comprising at least two rows, wherein each row comprises upper conductive segments and lower conductive segments, and in at least one row the upper conductive segments are longer than the lower conductive segments; and

mounting an integrated circuit on the substrate.

23. The integrated circuit package recited in claim 22 wherein, in forming the substrate, the substrate is formed of material from the group consisting of silicon, germanium, gallium arsenide, polyimide, organic material, a printed circuit board, glass, quartz, and ceramic.

24. The integrated circuit package recited in claim 22 wherein, in forming the at least one multi-level inductive element, the upper conductive segments and the lower conductive segments are arranged in a stepped manner.

25. The integrated circuit package recited in claim 22 wherein, in forming the at least one multi-level inductive element, the upper conductive segments and the lower conductive segments are arranged in an undulating manner.

26. The integrated circuit package recited in claim 22 wherein, in forming the at least one multi-level inductive element, the upper conductive segments in one row are offset 180 degrees from the upper conductive segments in an adjacent row.

27. The integrated circuit package recited in claim 22 wherein, in forming the at least one multi-level inductive element, the at least one multi-level inductive element comprises at least one layer of magnetic material.

28. An integrated circuit component fabricated by:

forming a silicon substrate; and

forming at least one multi-level inductive element on the substrate in a serpentine pattern comprising at least two rows, wherein each row comprises upper conductive segments and lower conductive segments, and in at least one row the upper conductive segments are longer than the lower conductive segments.

29. The integrated circuit component recited in claim 28 wherein, in forming the at least one multi-level inductive element, the upper conductive segments in one row are offset 180 degrees from the upper conductive segments in an adjacent row.

30. The integrated circuit component recited in claim 28 wherein, in forming the at least one multi-level inductive element, the at least one multi-level inductive element comprises at least one layer of magnetic material.

31. An integrated circuit fabricated by:

forming at least one multi-level inductive element on a substrate in a serpentine pattern comprising at least two rows, wherein each row comprises upper conductive

segments and lower conductive segments, and in at least one row the upper conductive segments are longer than the lower conductive segments.

32. The integrated circuit recited in claim 31 wherein, in forming, the upper conductive segments and the lower conductive segments are arranged in a stepped manner.

33. The integrated circuit recited in claim 31 wherein, in forming, the upper conductive segments and the lower conductive segments are arranged in an undulating manner.

34. The integrated circuit recited in claim 31 wherein, in forming, the upper conductive segments in one row are offset 180 degrees from the upper conductive segments in an adjacent row.

35. The integrated circuit recited in claim 31 wherein, in forming, the at least one multi-level inductive element comprises at least one layer of magnetic material.